19-3281; Rev 1; 1/05

MAXIM

-48V Hot-Swap Controllers with VIN Step Immunity and No RSENSE

General Description

The MAX5936/MAX5937 are hot-swap controllers for -10V to -80V rails. The MAX5936/MAX5937 allow circuit line cards to be safely hot-plugged into a live backplane without causing a glitch on the power supply. These devices integrate a circuit-breaker function requiring no R_{SENSE}.

The MAX5936/MAX5937 provide a controlled turn-on for circuit cards, limiting inrush, preventing glitches on the power-supply rail, and preventing damage to board connectors and components. Before startup, the devices perform a Load Probe™ test to detect the presence of a short-circuit condition. If a short-circuit condition does not exist, the device limits the inrush current drawn by the load by gradually turning on the external MOSFET. Once the external MOSFET is fully enhanced, the MAX5936/MAX5937 provides overcurrent and short-circuit protection by monitoring the voltage drop across the $R_{DS(ON)}$ of the external power MOSFET. The MAX5936/MAX5937 integrate a 400mA fast GATE pulldown to guarantee that the power MOSFET is rapidly turned off in the event of an overcurrent or short-circuit condition.

The MAX5936/MAX5937 protect the system against input voltage (V_{IN}) steps by providing V_{IN} step immunity. The MAX5936/MAX5937 provide an accurate UVLO voltage. The MAX5936 has an open-drain, active-low $\overline{PGOOD}$ output and the MAX5937 has an open-drain, active-high PGOOD output.

The MAX5936/MAX5937 are offered with 100mV, 200mV, and 400mV circuit-breaker thresholds, in addition to a non-circuit-breaker option. These devices are offered in latched and autoretry fault management, are available in 8-pin SO packages, and specified for the extended (-40°C to +85°C) temperature range (see the *Selector Guide*).

Applications

Servers

Telecom Line Cards

Network Switches

Solid-State Circuit Breaker

Network Routers

Load Probe is a trademark of Maxim Integrated Products, Inc.

Features

- **-10V to -80V Operation**
- **No R_{SENSE} Required**
- **Drives Large Power MOSFETS**
- **Programmable Inrush Current Limit During Hot Plug**
- **100mV, 200mV, 400mV, and No-Circuit-Breaker Threshold Options**
- **Circuit-Breaker Fault with Transient Rejection**
- **Shorted Load Detection (Load Probe) Before Power MOSFET Turn-On**
- **±2.4% Accurate Undervoltage Lockout (UVLO)**
- **Autoretry and Latched Fault Management Available**
- **Low Quiescent Current**

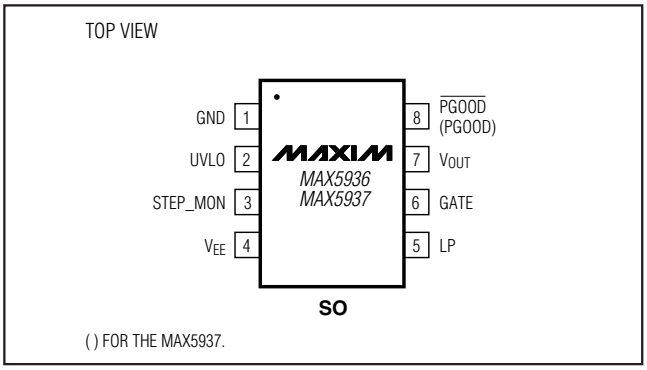
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5936_ _ESA	-40°C to +85°C	8 SO
MAX5937_ _ESA	-40°C to +85°C	8 SO

Note: *The first "_" represents A for the autoretry and L for the latched fault management option.*
The second "_" represents the circuit-breaker threshold.
See the Selector Guide for additional information.

Selector Guide and Typical Operating Circuit appear at end of data sheet.

Pin Configuration



-48V Hot-Swap Controllers with VIN Step Immunity and No RSENSE

ABSOLUTE MAXIMUM RATINGS

V_{EE}, V_{OUT}, PGOOD ($\overline{PGOOD}$), LP, STEP_MON to GND ..... +0.3V to -85V
PGOOD ($\overline{PGOOD}$) to V_{OUT} ..... -0.3V to +85V
PGOOD ($\overline{PGOOD}$), LP, STEP_MON to V_{EE} ..... -0.3V to +85V
GATE to V_{EE} ..... -0.3V to +20V
UVLO to V_{EE} ..... -0.3V to +6V
Input Current
LP (internally, duty-cycle limited) 1A
PGOOD ($\overline{PGOOD}$) (continuous) 80mA
GATE (during 15V clamp, continuous) 30mA
GATE (during 2V clamp, continuous) 50mA
GATE (during gate pulldown, continuous) 50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 5.9mW/°C above +70°C) 471mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = -10V to -80V, V_{IN} = GND - V_{EE}, V_{STEP_MON} = V_{EE}, R_{LP} = 200Ω, UVLO open, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{EE} = -48V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{EE}	Referenced to GND		-80		-10	V
Operating Supply Current	I_{CC}				0.95	1.4	mA
Default V_{EE} Undervoltage Lockout	$V_{UVLO,R}$	$\lvert V_{EE}\rvert$ increasing		-33.5	-31.0	-29.5	V
	$V_{UVLO,F}$	$\lvert V_{EE}\rvert$ decreasing			-28		
UVLO Reference Threshold, V_{EE} Rising	$V_{UVLO\_REF,R}$	V_{UVLO} increasing		1.219	1.25	1.281	V
UVLO Reference Threshold, V_{EE} Falling	$V_{UVLO\_REF,F}$	V_{UVLO} decreasing		1.069	1.125	1.181	V
UVLO Input Resistance				20		50	kΩ
UVLO Transient Rejection	t_{OVREJ}			0.8	1.5	2.25	ms
Power-Up Delay (Note 3)	t_{ONDLY}			80	220	380	ms
V_{EE} and UVLO Glitch Rejection (Note 4)	t_{REJ}			0.8	1.5	2.25	ms
V_{OUT} to V_{EE} Leakage Current		V_{EE} = -80V, V_{OUT} = GND			0.01	1	µA
LP to V_{EE} Leakage Current		V_{EE} = -80V, V_{LP} = GND			0.01	1	µA
External Gate-Drive Voltage	V_{GS}	V_{GATE} - V_{EE}	V_{IN} = 10V	6.5	6.8	7.2	V
			14 ≤ V_{IN} ≤ 80V	8.1	10	12.8	
GATE to V_{EE} Clamp Voltage		MOSFET fully enhanced	I_{CLAMP} = 9mA	13.5	16		V
			I_{CLAMP} = 20mA		17	19.5	
		Power-off, V_{EE} = GND	I_{CLAMP} = 1mA		2.1	2.55	
			I_{CLAMP} = 10mA		2.5	2.9	
Open-Loop Gate-Charge Current		V_{GATE} = V_{EE}, V_{OUT} = GND		-66	-52	-35	µA
GATE Pulldown Switch On-Resistance	R_{GATE}	V_{GATE} - V_{EE} = 500mV	V_{IN} > 10V		9	14.1	Ω
			V_{IN} > 14V		7.5	12.5	
Output-Voltage Slew Rate	SR	$\lvert dV_{OUT}/dt \rvert$		2.4	9	14.8	V/ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -10V to -80V, V_{IN} = GND - V_{EE}, V_{STEP_MON} = V_{EE}, R_{LP} = 200Ω, UVLO open, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{EE} = -48V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Circuit-Breaker Tempco		-40°C < T_A <+85°C			6000		ppm/°C
Circuit-Breaker Glitch Rejection	t_{CB_DLY}			1.0	1.2	1.6	ms
Circuit-Breaker Threshold	V_{CB}	MAX5936LA/ MAX5936AA/ MAX5937LA/ MAX5937AA	T_A = +85°C	118	140	162	mV
			T_A = +25°C	85	100	115	
			T_A = -10°C	64	79	94	
			T_A = -40°C		62		
		MAX5936LB/ MAX5936AB/ MAX5937LB/ MAX5937AB	T_A = +85°C	244	284	324	
			T_A = +25°C	180	200	220	
			T_A = -10°C	135	158	181	
			T_A = -40°C		124		
		MAX5936LC/ MAX5936AC/ MAX5937LC/ MAX5937AC	T_A = +85°C	485	568	651	
			T_A = +25°C	355	400	445	
			T_A = -10°C	270	316	362	
			T_A = -40°C		248		
Short-Circuit Threshold	V_{SC}	MAX5936LA/ MAX5936AA/ MAX5937LA/ MAX5937AA	T_A = +85°C	220	280	340	mV
			T_A = +25°C	160	200	240	
			T_A = -10°C	111	158	205	
			T_A = -40°C		124		
		MAX5936LB/ MAX5936AB/ MAX5937LB/ MAX5937AB	T_A = +85°C	470	568	667	
			T_A = +25°C	350	400	450	
			T_A = -10°C	255	316	377	
			T_A = -40°C		248		
		MAX5936LC/ MAX5936AC/ MAX5937LC/ MAX5937AC	T_A = +85°C	962	1136	1310	
			T_A = +25°C	700	800	900	
			T_A = -10°C	510	632	754	
			T_A = -40°C		496		
Short-Circuit Response Time (Note 5)		150mV overdrive, C_{LOAD} = 0, to GATE below 1V			330	500	ns
INPUT-VOLTAGE-STEP PROTECTION							
Input-Voltage-Step Detection Threshold	$STEP_{TH}$			1.219	1.250	1.281	V
Input-Voltage-Step Threshold Offset Current	I_{STEP_OS}			-10.8	-10.0	-9.2	µA
LOAD-PROBE CIRCUIT							
Load-Probe Switch On-Resistance		V_{LP} - V_{EE} = 1V			7.5	11	Ω
Load-Probe Timeout	t_{LP}			80	220	380	ms
Load-Probe Retry Time	t_{LP_OFF}				16 x t_{LP}		s
Load-Probe Voltage Threshold	$V_{THSC-DET}$	Referenced to GND		-220	-200	-180	mV

-48V Hot-Swap Controllers with VIN Step Immunity and No RSENSE

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -10V to -80V, V_{IN} = GND - V_{EE}, V_{STEP_MON} = V_{EE}, R_{LP} = 200Ω, UVLO open, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{EE} = -48V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC AND FAULT MANAGEMENT						
Autoretry Delay	t_{RETRY}			16 x t_{LP}		s
PGOOD ($\overline{PGOOD}$) Assertion Threshold		$\lvert V_{OUT} - V_{EE} \rvert$ falling		0.74 x V_{CB}		mV
		Hysteresis		0.26 x V_{CB}		
PGOOD ($\overline{PGOOD}$) Assertion Delay Time (Note 6)			0.67	1.26	1.85	ms
PGOOD ($\overline{PGOOD}$) Low Voltage	V_{OL}	I_{SINK} = 1mA, referenced to V_{OUT}, V_{OUT} < GND - 5V for PGOOD ($\overline{PGOOD}$)		0.05	0.4	V
PGOOD ($\overline{PGOOD}$) Open-Drain Leakage	I_L	V_{EE} = -80V, $V_{PGOOD(\overline{PGOOD})}$, $V_{PGOOD(\overline{PGOOD})}$ = GND		0.01	1	µA

Note 1: All currents into pins are positive and all currents out of pins are negative. All voltages referenced to V_{EE}, unless otherwise specified.

Note 2: All limits are 100% tested at +25°C and +85°C. Limits at -40°C and -10°C are guaranteed by characterization.

Note 3: Delay time from a valid on-condition until the load probe test begins.

Note 4: V_{EE} or UVLO voltages below $V_{UVLO,F}$ or $V_{UVLO\_REF,F}$, respectively, are ignored during this time.

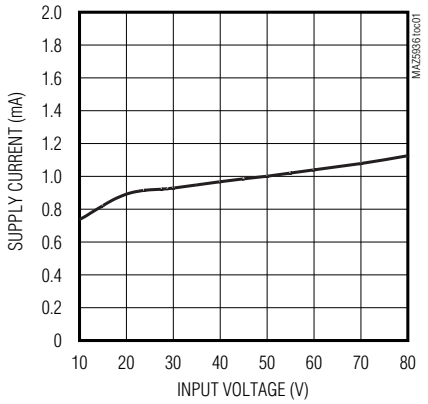
Note 5: The time (V_{OUT} - V_{EE}) > V_{SC} + overdrive until (V_{GATE} - V_{EE}) drops to approximately 90% of its initial high value.

Note 6: The time when the PGOOD ($\overline{PGOOD}$) condition is met until the PGOOD ($\overline{PGOOD}$) signal is asserted.

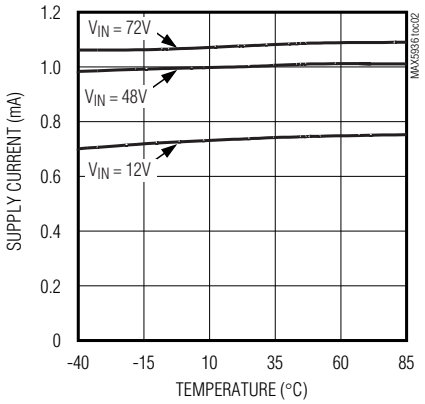
Typical Operating Characteristics

(V_{EE} = -48V, GND = 0V, V_{IN} = GND - V_{EE}, all voltages are referenced to V_{EE}, T_A = +25°C, unless otherwise noted.)

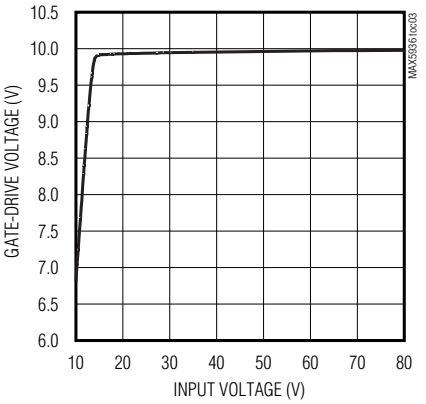
SUPPLY CURRENT vs. INPUT VOLTAGE



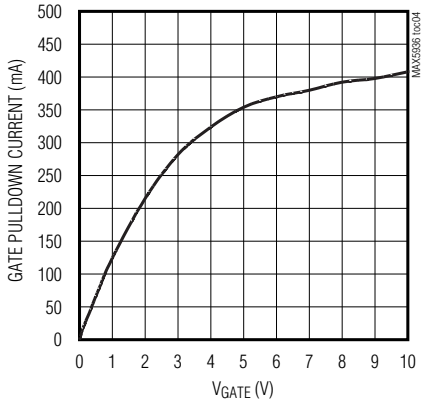
SUPPLY CURRENT vs. TEMPERATURE



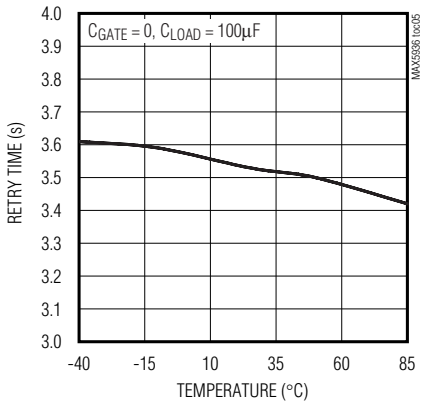
GATE-DRIVE VOLTAGE vs. INPUT VOLTAGE



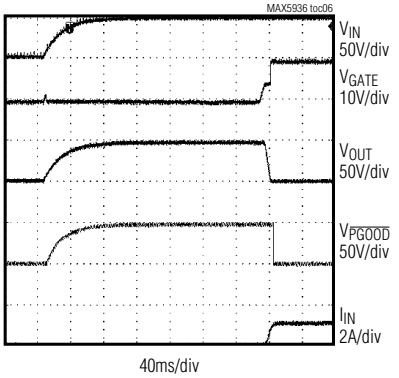
GATE PULLDOWN CURRENT vs. GATE VOLTAGE



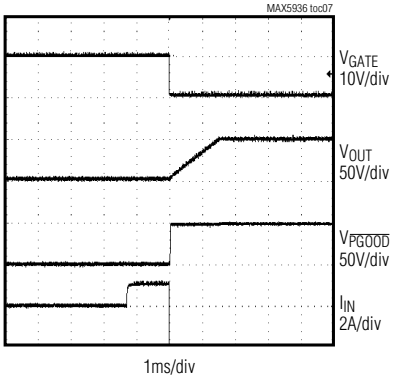
RETRY TIME vs. TEMPERATURE



STARTUP WAVEFORM



MAX5936_A CIRCUIT-BREAKER EVENT

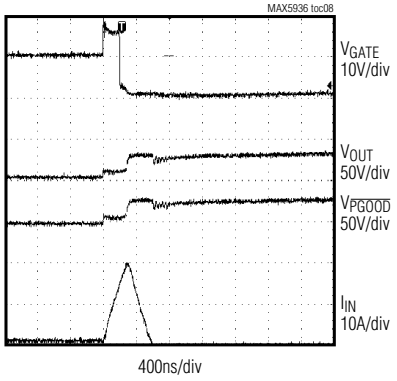


-48V Hot-Swap Controllers with V_{IN} Step Immunity and No R_{SENSE}

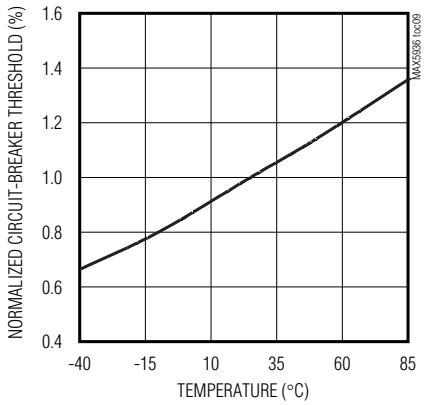
Typical Operating Characteristics (continued)

(V_{EE} = -48V, GND = 0V, V_{IN} = GND - V_{EE}, all voltages are referenced to V_{EE}, T_A = +25°C, unless otherwise noted.)

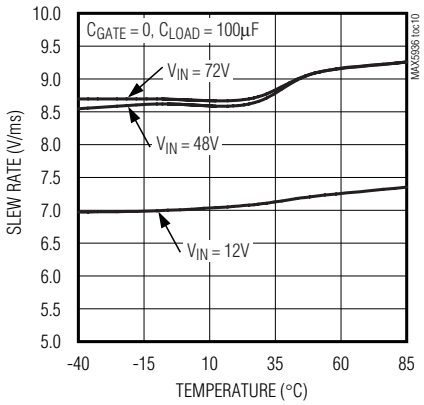
MAX5936_A SHORT-CIRCUIT EVENT



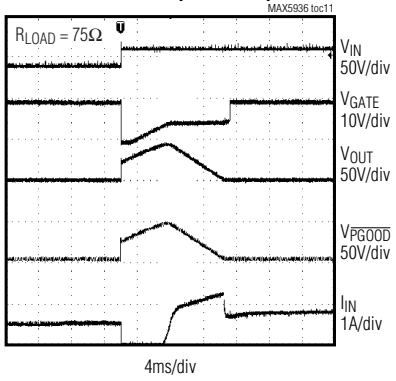
NORMALIZED CIRCUIT-BREAKER THRESHOLD vs. TEMPERATURE



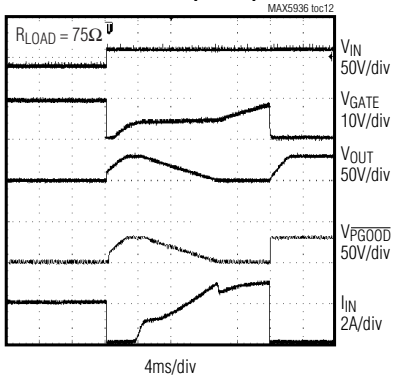
V_{OUT} SLEW RATE vs. TEMPERATURE



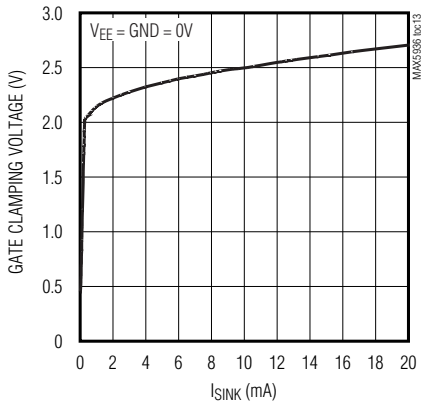
MAX5936_A INPUT VOLTAGE STEP EVENT (NO FAULT)



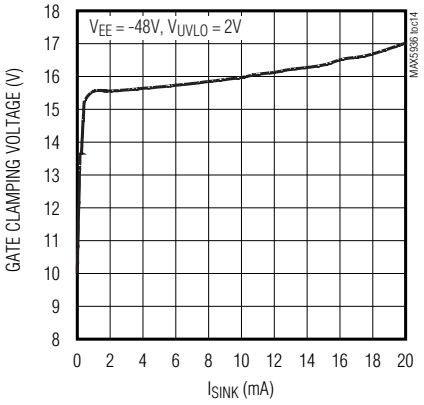
MAX5936_A INPUT VOLTAGE STEP EVENT (FAULT)



GATE TO V_{EE} CLAMP VOLTAGE AT POWER OFF



GATE TO V_{EE} CLAMP VOLTAGE MOSFET FULLY ENHANCED



Pin Description

PIN		NAME	FUNCTION
MAX5936	MAX5937		
1	1	GND	Ground. The high-supply connection for a negative-rail hot-swap controller.
2	2	UVLO	Undervoltage Lockout Input, On/Off Control. Referenced to V_{EE}. Drive UVLO above the 1.25V rising threshold to turn on the device. To turn off the device, drive UVLO below the 1.125V falling threshold for the 1.5ms glitch rejection period. Leave UVLO disconnected for the default 31V undervoltage lockout threshold. Cycle UVLO to unlatch the MAX5936L/MAX5937L after a fault. Cycling UVLO low deasserts PGOOD.
3	3	STEP_MON	Input Voltage Step Monitor. 1.25V voltage threshold referenced to V_{EE}. Connect a resistor between STEP_MON and V_{EE} to set the step sensitivity. Connect a capacitor from GND to STEP_MON to adjust the step response relative to a step increase at V_{EE} to eliminate false circuit-breaker and short-circuit faults. Connect to V_{EE} to disable the step immunity function (see the *Selecting Resistor and Capacitor Values for Step Monitor* section in the *Applications Information*).
4	4	V_{EE}	Negative Input Voltage
5	5	LP	Load-Probe Detect. Connect a resistor from LP to V_{OUT} to set the load-probe test current. **Limit load-probe test current to 1A.** Connect to V_{EE} to disable the load-probe function.
6	6	GATE	Gate-Drive Output. Connect to the gate of the external n-channel MOSFET.
7	7	V_{OUT}	Output Voltage Sense. V_{OUT} is the negative rail of the load. Connect to the drain of the external n-channel MOSFET.
8	—	$\overline{PGOOD}$	Power-Good, Active-Low, Open-Drain Output. Referenced to V_{OUT}. $\overline{PGOOD}$ asserts low when V_{OUT} is within the limits and there is no fault.
—	8	PGOOD	Power-Good, Active-High, Open-Drain Output. Referenced to V_{OUT}. PGOOD asserts high when V_{OUT} is within limits and there is no fault.

Detailed Description

The MAX5936/MAX5937 hot-swap controllers incorporate overcurrent fault management and are intended for negative-supply-rail applications. The MAX5936/MAX5937 eliminate the need for an external R_{SENSE} and include V_{IN} input-step protection and load probe, which prevents powering up into a shorted load. They are intended for negative 48V telecom power systems where low cost, flexibility, multifault management, and compact size are required. The MAX5936/MAX5937 are ideal for the widest range of systems from those requiring low current with small MOSFETs to high-current systems requiring large power MOSFETs and low on-resistance.

The MAX5936/MAX5937 control an external n-channel power MOSFET placed in the negative supply path of an external load. When no power is applied, the GATE output of the MAX5936/MAX5937 clamps the V_{GS} of the MOSFET to 2V, keeping the MOSFET turned off. When power is applied to the MAX5936/MAX5937, the 2V clamp at the GATE output is replaced by a strong pull-down device pulling GATE to V_{EE} and the V_{GS} of the MOSFET to 0V. As shown in Figure 2, this transition enables the MAX5936/MAX5937 to keep the power MOSFET continually off during the board insertion phase when the circuit board first makes contact with the backplane. Without this clamp, the GATE output of a powered-down controller would be floating and the MOSFET reverse transfer capacitance (gate-to-drain) would pull up and turn on the MOSFET gate when the MOSFET drain is rapidly pulled up by the V_{IN} step during backplane contact. The MAX5936/MAX5937 GATE clamp can overcome the gate-to-drain capacitance of large power MOSFETs with added slew-rate control (C_{SLEW}) capacitors while eliminating the need for additional gate-to-source capacitance. The MAX5936/MAX5937 will keep the MOSFET off indefinitely if the supply voltage is below the user-set UVLO threshold or if a short circuit is detected in the load connected to the drain of the power MOSFET.

-48V Hot-Swap Controllers with V_{IN} Step Immunity and No R_{SENSE}

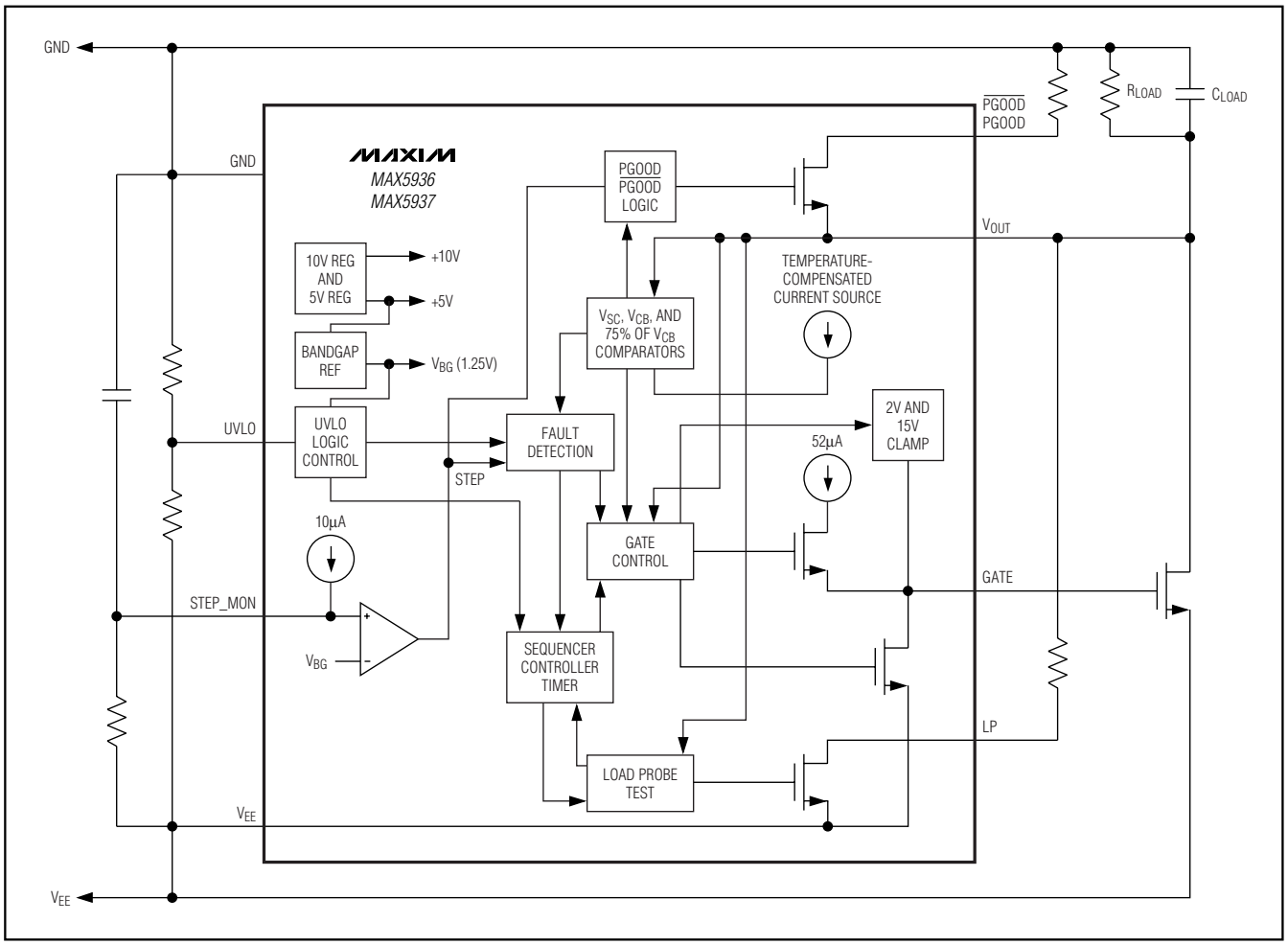


Figure 1. Functional Block Diagram

The MAX5936/MAX5937 conduct a load-probe test after contact transients from the hot plug-in have settled. This follows the MAX5936/MAX5937 power-up (when the UVLO condition has been met for 220ms (t_{LP})) and prior to the turn-on of the power MOSFET. This test pulls a user-programmable current through the load (1A, max) for up to 220ms and tests for a voltage of 200mV across the load at V_{OUT}. This current is set by an external resistor, R_{LP}, between V_{OUT} and LP (Figure 14). When the voltage across the load exceeds 200mV, the test is truncated and the GATE turn-on sequence is started. If at the end of the 220ms test period the voltage across the load has not reached 200mV, the load is assumed to be shorted and the current to the load from the LP pin is shut off. The MAX5936A_/MAX5937A_ will timeout for 16 x t_{LP} then retry the load-probe test. The MAX5936L_/MAX5937L_ will latch the fault condition indefinitely until the UVLO is brought below 1.125V for 1.5ms or the power is recycled. See the *Applications Information* section for recommendations on selecting R_{LP} to set the current level.

Upon successful completion of the load-probe test, the MAX5936/MAX5937 enter the power-up GATE cycle and begin ramping the GATE voltage with a 52µA current source. This current source is restricted if V_{OUT} begins to ramp down faster than the default 9V/ms slew rate. Charging up GATE enhances the power MOSFET in a controlled manner and ramping V_{OUT} at a user-settable rate controls the inrush current from the backplane. The MAX5936/MAX5937 continue to charge up the GATE until one of two events occurs: a normal power-up GATE cycle is completed or a power-up to fault management is detected (see the *GATE Cycles* section in *Appendix A*).

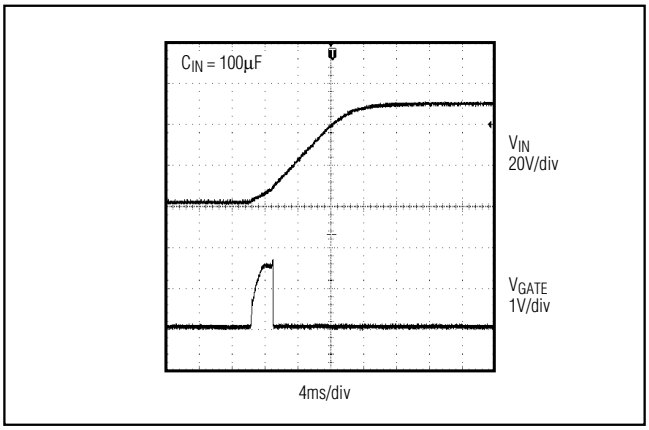


Figure 2. GATE Voltage Clamp During Power-Up

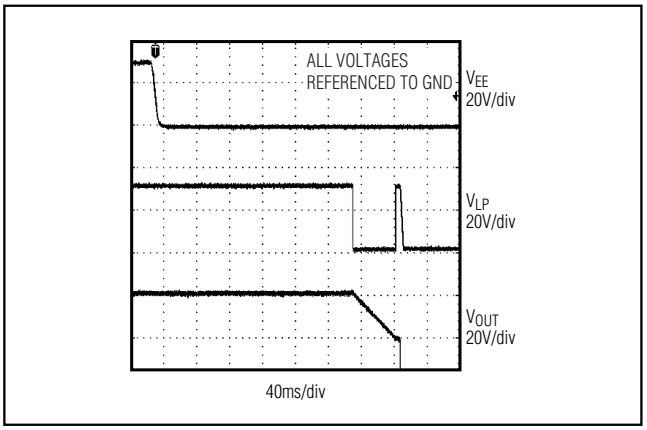


Figure 3. Load Probe Test During Initial Power-Up

In a normal power-up GATE cycle, the voltage at V_{OUT} (referenced to V_{EE}) ramps to below 74% of the circuit-breaker threshold voltage, V_{CB}. At this time, the remaining GATE voltage is rapidly pulled up to full enhancement. PGOOD is asserted 1.26ms after GATE is fully enhanced (see Figure 4). If the voltage at V_{OUT} remains above 74% of the V_{CB} (when GATE reaches 90% of full enhancement), then a power-up to fault management fault has occurred (see Figure 5). GATE is rapidly pulled to V_{EE}, turning off the power MOSFET and disconnecting the load. PGOOD remains deasserted and the MAX5936/MAX5937 enter the fault management mode.

When the power MOSFET is fully enhanced, the MAX5936/MAX5937 monitor the drain voltage (V_{OUT}) for circuit-breaker and short-circuit faults. The MAX5936/MAX5937 make use of the power MOSFET's $R_{DS(ON)}$ as the current-sense resistance to detect excessive current through the load. The short-circuit threshold voltage, V_{SC}, is twice V_{CB} (V_{SC} = 2 x V_{CB}) and is available in 100mV, 200mV, and 400mV thresholds. V_{CB} and V_{SC} are temperature-compensated (increasing with temperature) to track the normalized temperature coefficient of $R_{DS(ON)}$ for typical power MOSFETs.

When the load current is increased during full enhancement, this causes V_{OUT} to exceed V_{CB} but remains less than V_{SC}, and starts the 1.2ms circuit-breaker glitch rejection timer. At the end of the glitch rejection period, if V_{OUT} still exceeds V_{CB}, the $\overline{GATE}$ is immediately pulled to V_{EE} (330ns), PGOOD ($\overline{PGOOD}$) is deasserted, and the part enters fault management. Alternatively, during full enhancement when V_{OUT} exceeds V_{SC}, there is no glitch rejection timer. GATE is immediately pulled to V_{EE}, PGOOD is deasserted, and the part enters fault management.

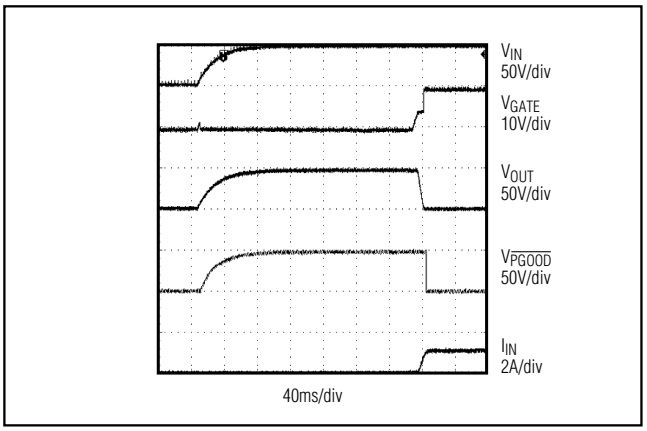


Figure 4. MAX5936 Normal Condition

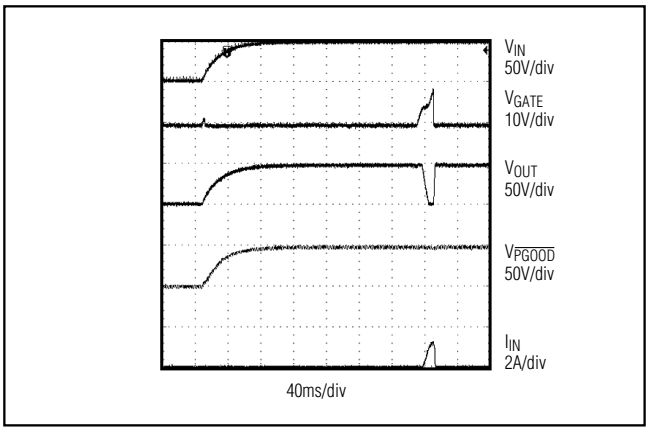


Figure 5. MAX5936 Startup in Fault Condition

-48V Hot-Swap Controllers with V_{IN} Step Immunity and No R_{SENSE}

The V_{IN} step immunity provides a means for transitioning through a large step increase in V_{IN} with minimal backplane inrush current and without shutting down the load. Without V_{IN} step immunity (when the power MOSFET is fully enhanced), a step increase in V_{IN} will result in a high inrush current and a large step in V_{OUT}, which can trip the circuit breaker. With V_{IN} step immunity, the STEP_MON input detects the step before a short circuit is detected at V_{OUT} and alters the MAX5936/MAX5937 response to V_{OUT} exceeding V_{SC} due to the step. The 1.25V voltage threshold at STEP_MON and a 10µA current source at STEP_MON allow the user to set the sensitivity of the step detection with an external resistor to V_{EE}. A capacitor is placed between GND and the STEP_MON input, which, in conjunction with the resistor, sets the STEP_MON time constant. When a step is detected by the STEP_MON input to rise above its threshold ($STEP_{TH}$), the overcurrent fault management is blocked and remains blocked as long as $STEP_{TH}$ is exceeded. When $STEP_{TH}$ is exceeded, the MAX5936/MAX5937 take no action until V_{OUT} rises above V_{SC} or above V_{CB} for the 1.2ms circuit-breaker glitch rejection period. When either of these conditions occurs, a step GATE cycle begins and the GATE is immediately brought to V_{EE}, which turns off the power MOSFET to minimize the resulting inrush current surge from the backplane and PGOOD remains asserted. GATE is held at V_{EE} for 350µs, and after about 1ms, begins to ramp up thereby enhancing the power MOSFET in a controlled manner as in the power-up GATE cycle. This provides a controlled inrush current to charge the load capacitance to the new supply voltage (see the *GATE Cycles* section in *Appendix A*).

As in the case of the power-up GATE cycle, if V_{OUT} drops to less than 74% of the programmed V_{CB}, independent of the state of STEP_MON, the GATE voltage is rapidly pulled to full enhancement. PGOOD remains asserted throughout the step. Otherwise, if the STEP_MON input has decayed below its threshold but V_{OUT} remains above 74% of the programmed V_{CB} (when GATE reaches 90% of full enhancement), (a step-to-fault management fault has occurred). GATE is rapidly pulled to V_{EE}, turning off the power MOSFET and disconnecting the load, PGOOD ($\overline{PGOOD}$) is deasserted, and the MAX5936/MAX5937 enter the fault management mode.

Fault Management

Fault management can be triggered by the following conditions:

- V_{OUT} exceeds 74% of V_{CB} during GATE ramp at 90% of full enhancement,
- V_{OUT} exceeds the V_{CB} for longer than 1.2ms during full enhancement,
- V_{OUT} exceeds the V_{SC} during full enhancement, and
- Load-probe test fails.

Once in the fault management mode, GATE will always be pulled to V_{EE} to turn off the external MOSFET and PGOOD ($\overline{PGOOD}$) will always be deasserted. The MAX5936A_/MAX5937A_ have automatic retry following a fault while the MAX5936L_/MAX5937L remain latched in the fault condition.

Autoretry Fault Management (MAX5936A_/MAX5937A_)

If the MAX5936A_/MAX5937A_entered fault management due to circuit-breaker and short-circuit faults, the autoretry timer starts immediately. The timer times out in 3.5s (typ) and at the end of the timeout, the sequencer initiates a load-probe test. If this is successful, it starts a normal power-up GATE cycle.

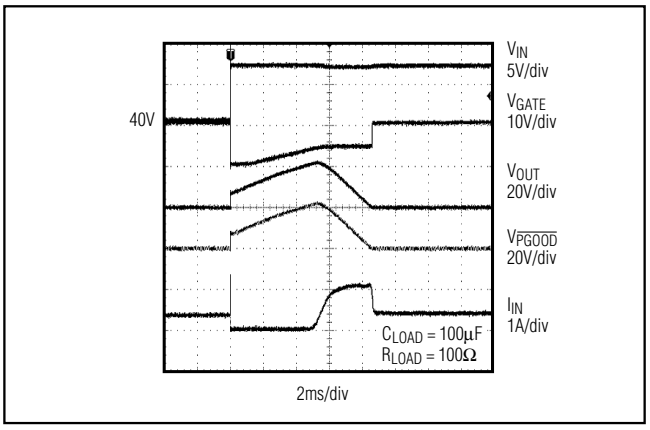


Figure 6. MAX5936 Response to a Step Input (V_{OUT} < 0.74V_{CB})

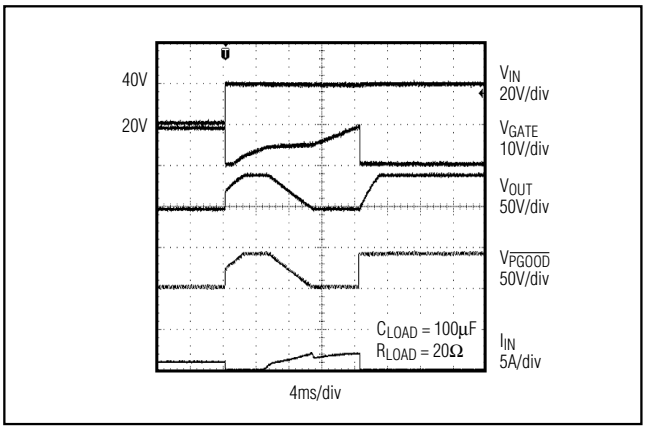


Figure 7. MAX5936 Response to a Step Input (V_{OUT} > 0.74V_{CB})

Latched Fault Management (MAX5936L_/MAX5937L_)

When the MAX5936L_/MAX5937L_ enter fault management, they remain in this condition indefinitely until the power is recycled or until UVLO is brought below 1.125V for 1.5ms (typ) (when the short-circuit or circuit-breaker fault has cleared, the sequencer initiates a load-probe test). If this is successful, it starts a normal power-up GATE cycle. A manual reset circuit (Figure 8) can be used to clear the latch.

Circuit-Breaker Thresholds

The MAX5936/MAX5937 are available with 100mV, 200mV, and 400mV circuit-breaker thresholds. The short-circuit voltage threshold (V_{SC}) is twice the circuit-breaker threshold voltage (V_{CB}). In the MAX5936/MAX5937, V_{CB} and V_{SC} are temperature-compensated (increasing with temperature) to track the normalized temperature gradient of typical power MOSFETs.

The proper circuit-breaker threshold for an application depends on the $R_{DS(ON)}$ of the external power MOSFET and the maximum current the load is expected to draw. To avoid false fault indication and dropping of the load, the designer must take into account the load response to voltage ripples and noise from the backplane power supply, as well as switching currents in the downstream DC-DC converter that is loading the circuit. While the circuit-breaker threshold has glitch rejection that ignores ripples and noise lasting less than 1.2ms, the short-circuit detection is designed to respond very quickly (less than 330ns) to a short circuit. V_{SC} and V_{CB} must be selected from the three available ranges with an adequate margin to cover all possible ripples, noise, and system current transients.

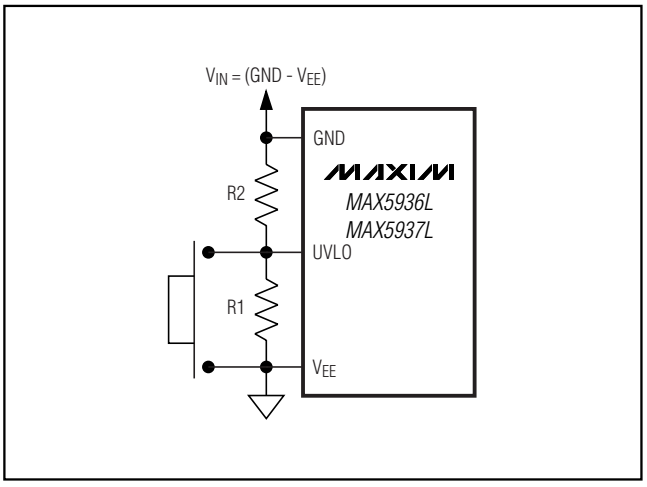


Figure 8. Resetting MAX5936L/MAX5937L after a Fault Condition Using a Push-Button Switch

The short-circuit and circuit-breaker voltages are sensed at V_{OUT}, which is the drain of the power MOSFET. The $R_{DS(ON)}$ of the MOSFET is the current-sense resistance, so the total current through the load and load capacitance is the drain current of the power MOSFET. Accordingly, the voltage at V_{OUT} as a function of MOSFET drain current is:

$$V_{OUT} = I_{D,MOSFET} \times R_{DS(ON)}$$

The temperature compensation of the MAX5936/MAX5937 is designed to track the $R_{DS(ON)}$ of the typical power MOSFET. Figure 9 shows the typical normalized tempco of the circuit-breaker threshold along with the normalized tempco of $R_{DS(ON)}$ for two typical power MOSFETS. When determining the circuit-breaker threshold in an application, go to the data sheet of the power MOSFET and locate the manufacturer's maximum $R_{DS(ON)}$ at +25°C with a V_{GS} of 10V. Next, find the figure presenting the tempco of normalized $R_{DS(ON)}$ or on-resistance vs. temperature. Because this curve is in normalized units typically with a value of 1 at +25°C, it is possible to multiply the curve by the drain voltage at +25°C and convert the curve to drain voltage. Now compare this curve to that of the MAX5936/MAX5937 normalized tempco of the circuit-breaker threshold to make a determination of the tracking error in mV between the power MOSFET [$I_{D,MOSFET} \times R_{DS(ON)}$] and the MAX5936/MAX5937 over the application's operating temperature range. If the tempco of the power MOSFET is greater than that of the MAX5936/MAX5937, then additional margin will be required in selecting the circuit-breaker and short-circuit voltages at higher temperatures as compared to +25°C. When dissipation in the power MOSFET is expected to lead to local temperature elevation relative to ambient conditions, then it becomes imperative that the MAX5936/MAX5937 be located as close as possible to the power MOSFET. The marginal effect of temperature differences on circuit-breaker and short-circuit voltages can be estimated from a comparative plot such as Figure 9.

MAX5936LN and MAX5937LN

The MAX5936LN and MAX5937LN do not have circuit-breaker and short-circuit thresholds and these faults are ignored. For these devices PGOOD ($\overline{PGOOD}$) asserts 1.26ms after GATE has ramped to 90% of full enhancement. The step detection function of the MAX5936LN and MAX5937LN responds to V_{IN} and V_{OUT} steps with the same voltage thresholds as the MAX5936_C and MAX5937_C.

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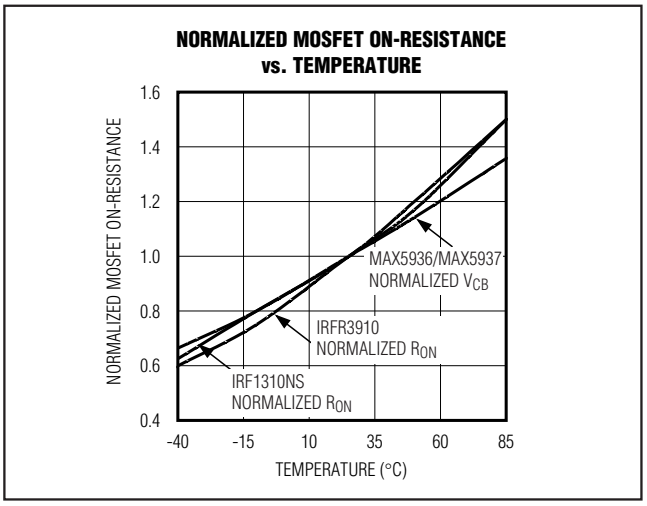

Figure 9. MAX5936/MAX5937 Normalized Circuit-Breaker Threshold (V_{CB})

PGOOD ($\overline{PGOOD}$) Open-Drain Output

The power-good outputs, PGOOD ($\overline{PGOOD}$), are open drain and are referenced to V_{OUT}. They assert and latch if V_{OUT} ramps below 72% of V_{CB}, and with the built-in delay this occurs 1.26ms after the external MOSFET becomes fully enhanced. PGOOD ($\overline{PGOOD}$) deasserts any time the part enters fault management. PGOOD ($\overline{PGOOD}$) has a delayed response to UVLO. The GATE goes to V_{EE} when UVLO is brought below 1.125V for 1.5ms. This turns off the power MOSFET and allows V_{OUT} to rise depending on the RC time constant of the load. PGOOD ($\overline{PGOOD}$), in this situation, deasserts when V_{OUT} rises above V_{CB} for more than 1.4ms or above V_{SC}, whichever occurs first (see Figure 12b).

Due to the open-drain driver, PGOOD ($\overline{PGOOD}$) requires an external pullup resistor to GND. Due to this external pullup, PGOOD will not follow positive V_{IN} steps as well as if it were driven by an active pullup. As a result, when PGOOD ($\overline{PGOOD}$) is asserted high, an apparent negative glitch appears at PGOOD ($\overline{PGOOD}$) during a positive V_{IN} step. This negative glitch is a result of the RC time constant of the external resistor and the PGOOD pin capacitance lagging the V_{IN} step. It is not due to switching of the internal logic. To minimize this negative transient, it may be necessary to increase the pullup current and/or to add a small amount of capacitance from PGOOD ($\overline{PGOOD}$) to GND to compensate for the pin capacitance.

WARNING: For the MAX5936_N/MAX5937_N, PGOOD ($\overline{PGOOD}$) asserts 1.26ms after the power MOSFET is fully enhanced, independent of V_{OUT}. Once the MOSFET is fully enhanced and UVLO is pulled below its respective threshold, GATE pulls to V_{EE} to turn off the power MOSFET and disconnect the load. When UVLO is cycled low, PGOOD ($\overline{PGOOD}$) is deasserted. In summary, once the MOSFET is fully enhanced, the MAX5936_N/ MAX5937_N ignore V_{OUT} and deassert PGOOD ($\overline{PGOOD}$) when UVLO goes low or when the power to the MAX5936_N/ MAX5937_N is fully recycled.

Undervoltage Lockout (UVLO)

UVLO provides an accurate means to set the turn-on voltage level for the MAX5936/MAX5937. Use a resistor-divider network from GND to V_{EE} to set the desired turn-on voltage (Figure 11). UVLO has hysteresis with a rising threshold of 1.25V and a falling threshold of 1.125V. A startup delay of 220ms allows contacts and voltages to settle prior to initiating the startup sequence (Figure 12a).

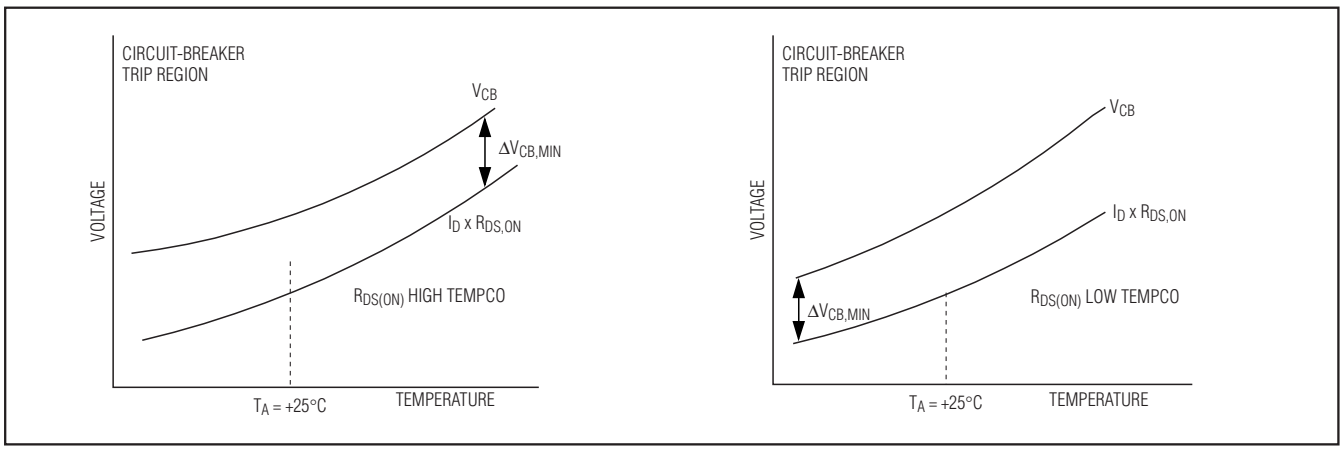

Figure 10. Circuit-Breaker Voltage Margin for High and Low Tempco Power MOSFETS

This startup delay is from a valid UVLO condition until the start of the load-probe test. There is glitch rejection on UVLO going low, which requires that V_{UVLO} remains below its falling threshold for 1.5ms to turn off the part (Figure 12b). Use the following formula to calculate the MAX5936/MAX59337 turn-on voltage:

$$R2 = \left(\frac{V_{ON}}{V_{UVLO\_REF,R}} - 1 \right) \times R1$$

Where V_{ON} is the desired turn-on voltage of the MAX5936/MAX5937 and $V_{UVLO\_REF,R}$ is the 1.25V UVLO rising threshold.

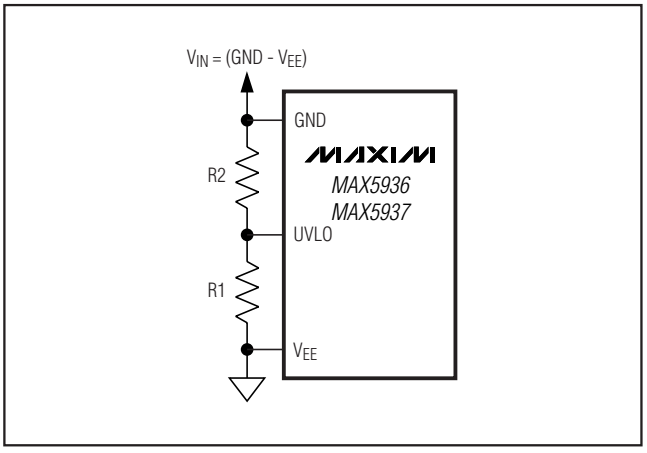

Figure 11. Setting the MAX5936/MAX5937 Turn-On Voltage

Output Voltage (VOUT) Slew-Rate Control

The V_{OUT} slew rate controls the inrush current required to charge the load capacitor. The MAX5936/MAX5937 have a default internal slew rate set for 9V/ms. The internal circuit establishing this slew rate accommodates up to about 1000pF of reverse transfer capacitance (miller capacitance) in the external power MOSFET without effecting the default slew rate. Using the default slew rate, the inrush current required to charge the load capacitance is given by:

$$I_{INRUSH}\ (mA) = C_{LOAD}\ (\mu F) \times SR\ (V/ms)$$

where SR = 9V/ms (default, typ).

Applications Information

Selecting Resistor and Capacitor for Step Monitor

When a positive V_{IN} step or ramp occurs, the V_{IN} increase results in a voltage rise at both STEP_MON and V_{OUT} relative to V_{EE}. When the voltage at STEP_MON is above $STEP_{TH}$ the MAX5936/MAX5937 block short-circuit and circuit-breaker faults. During this STEP_MON high condition, if V_{OUT} rises above V_{SC}, the MAX5936/MAX5937 immediately and very rapidly pull GATE to V_{EE}. This turns off the power MOSFET to avoid inrush current spiking. GATE is held low for 350µs. About 1ms after the start of GATE pulldown, the MAX5936/MAX5937 begin to ramp GATE up to turn on the MOSFET in a controlled manner, which results in ramping V_{OUT} down to the new supply level (see the *GATE Cycles* section in *Appendix A*).

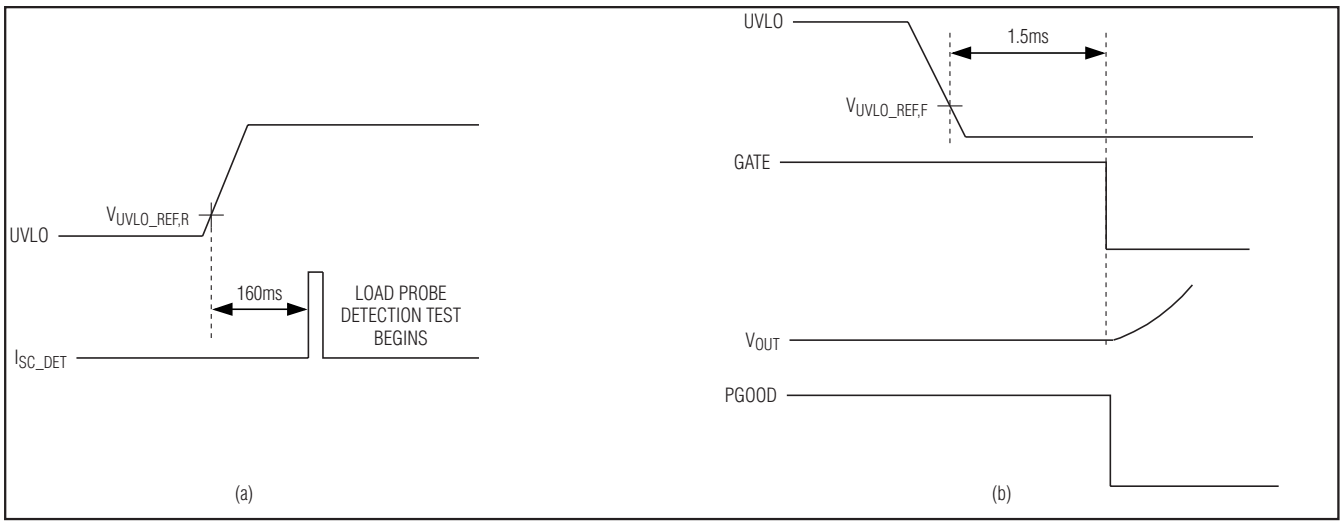

Figure 12. UVLO Timing Diagram

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This occurs with the least possible disturbance to V_{OUT}, although during the brief period that the MOSFET is off, the voltage across the load droops slightly depending on the load current and load storage capacitance. PGOOD remains asserted throughout the V_{IN} step event.

The objective in selecting the resistor and capacitor for the step monitor function is to ensure that the V_{IN} steps of all anticipated slopes and magnitudes will be properly detected and blocked, which otherwise would result in a circuit-breaker or short-circuit fault. The following is a brief analysis for finding the resistor and capacitor. For a more complete analysis, see *Appendix B*.

Figure 13 is a functional diagram exhibiting the elements of the MAX5936/MAX5937 involved in the step immunity function. This block diagram shows the parallel relationship between V_{OUT} and $V_{STEP-MON}$. Each has an I*R component establishing the DC level prior to a step. While it is referred to as a V_{IN} step, it is the dynamic response to a finite voltage ramp that is of interest.

Given a positive V_{IN} ramp with a ramp rate of dV/dt, the approximate response of V_{OUT} to V_{IN} is:

$$V_{OUT}(t) = (dV/dt) \times \tau_C \times (1-e^{(-t / \tau_{L,eqv})}) + R_{DS(ON)} \times I_{LOAD}$$

where $\tau_C = C_{LOAD} \times R_{DS(ON)}$ and $\tau_{L,eqv}$ is the equivalent time constant of the load that must be found empirically (see *Appendix B*).

Similarly, the response of STEP_MON to a V_{IN} ramp is:

$$V_{STEP\_MON}(t) = (dV/dt) \times \tau_{STEP} \times (1-e^{(-t / \tau STEP)}) + 10\mu A \times R_{STEP}$$

where $\tau_{STEP} = R_{STEP\_MON} \times C_{STEP\_MON}$.

For proper step detection, V_{STEP_MON} must exceed $STEP_{TH}$ prior to V_{OUT} reaching V_{SC} or within 1.4ms of V_{OUT} reaching V_{CB} (overall V_{IN} ramp rates anticipated in the application). V_{STEP_MON} must be set below $STEP_{TH}$ with adequate margin, ΔV_{STEP_MON}, to accommodate the tolerance of both I_{STEP_OS} (±8%) and R_{STEP_MON}. R_{STEP_MON} is typically set to 100kΩ which gives a ΔV_{STEP_MON} for a worst-case high of 0.36V.

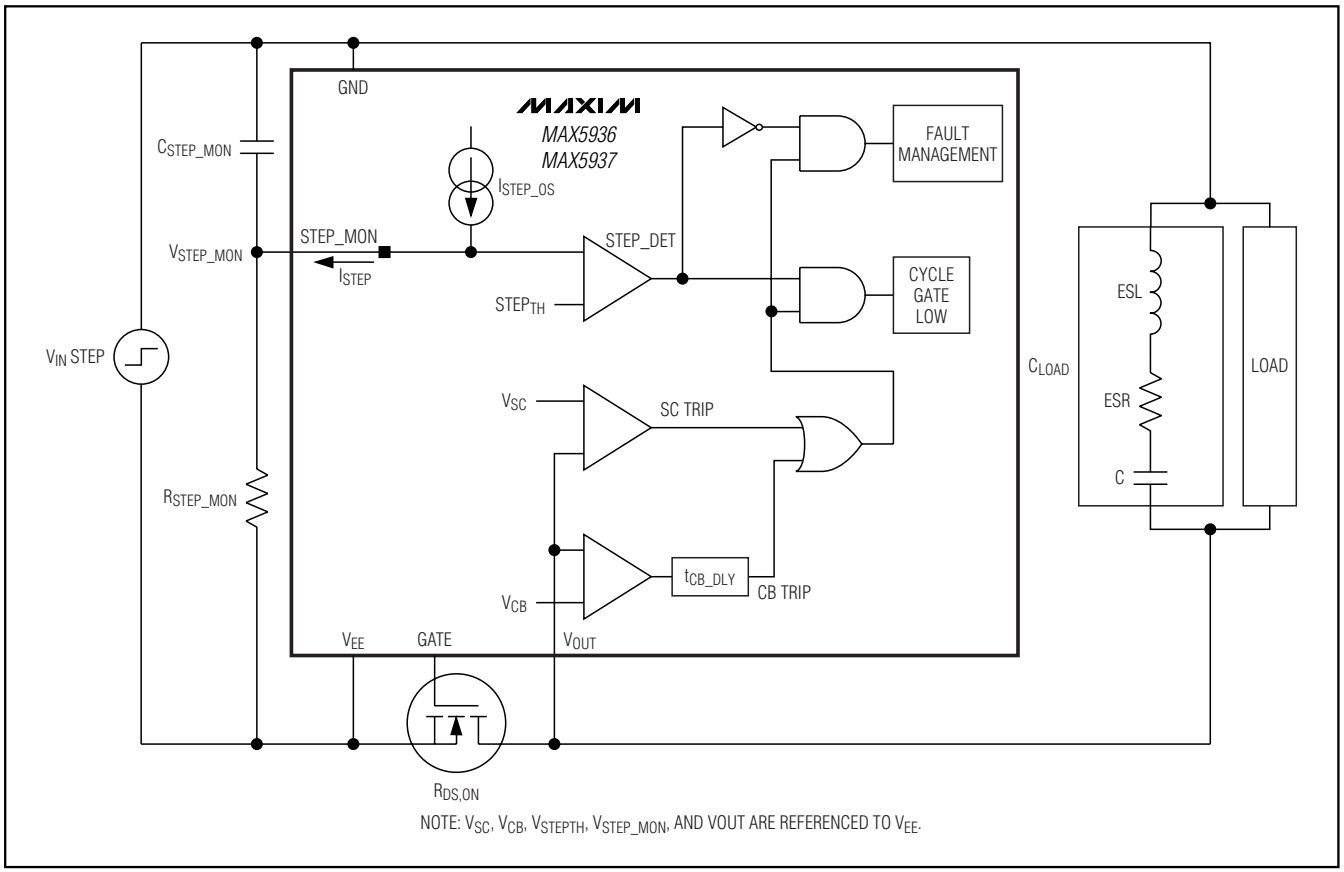

Figure 13. MAX5936/MAX5937 Step Immunity Functional Diagram

The margin of V_{OUT} with respect to V_{SC} and V_{CB} was set when V_{SC} and V_{CB} were selected from the three available ranges. This margin may be lower at one of the temperature extremes and if so, that value should be used in the following discussion. These margins will be called ΔV_{CB} and ΔV_{SC} and they represent the minimum V_{OUT} excursion required to trip the respective fault.

To set τ_{STEP} to block all V_{CB} and V_{SC} faults for any ramp rate, find the ratio of ΔV_{STEP_MON} to ΔV_{CB} and choose τ_{STEP} so:

$$\tau_{STEP} = 1.2 \times \tau_C \times \Delta V_{STEP\_MON} / \Delta V_{CB}$$

And since $R_{STEP\_MON} = 100k\Omega$. This results in $C_{STEP\_MON} = \tau_{STEP} / 100k\Omega$.

After the first-pass component selection, if sufficient timing margin exists (see *Appendix B*), it is possible but not necessary to lower R_{STEP_MON} below $100k\Omega$ to reduce the sensitivity of STEP_MON to V_{IN} noise.

Appendix B gives a more complete analysis and discussion of the step monitor function. It provides methods for the characterization of the load response to a V_{IN} ramp and graphical verification of the step monitor timing margins for a set of design parameters.

Selecting the PGOOD ($\overline{PGOOD}$) Pullup Resistor

Due to the open-drain driver, PGOOD ($\overline{PGOOD}$) requires an external pullup resistor to GND. This resistor should be selected to minimize the current load while PGOOD ($\overline{PGOOD}$) is low. The PGOOD output specification for V_{OL} is 0.4V at 1mA. As described in the *Detailed Description*, the external pullup interferes with the ability of PGOOD ($\overline{PGOOD}$) to follow positive V_{IN} steps as well as if it were driven by an active pullup. When PGOOD ($\overline{PGOOD}$) is asserted high, an apparent negative glitch appears at PGOOD during a positive V_{IN} step. To minimize this negative transient it may be necessary to increase the pullup current and/or to add a small amount of capacitance from PGOOD ($\overline{PGOOD}$) to GND to compensate for the pin capacitance.

Setting the Test Current Level for Load-Probe Test

The load-probe test is a current test of the load that avoids turning on the power MOSFET. The MAX5936/MAX5937 have an internal switch (Q1 in Figure 14) that pulls current through the load and through an external current-limiting resistor, R_{LP}. During the test, this switch is pulsed on for up to 220ms (typ). Current is pulled through the load, which should charge up the load capacitance unless there is a short. If the voltage across the load exceeds 200mV, the test is truncated and normal power-up is allowed to proceed. If the voltage across the load does not reach 200mV in the 220ms period that the current is on, the load is assumed to be shorted and the current to the load from the LP pin is shut off. The MAX5936A_/MAX5937A_ time out for 16 x t_{LP} then retry the load-probe test. The MAX5936L_/MAX5937L_ latch the fault condition indefinitely until the UVLO is brought below 1.125V for 1.5ms or the power is recycled.

In the application, the current-limiting resistor should be selected to minimize the current pulled through the load while guaranteeing that it charges the maximum expected load capacitance to 220mV in 80ms. These parameters are the maximum load-probe test voltage and the minimum load-probe current pulse period, respectively. The maximum current possible is 1A, which is adequate to test a load capacitance as large as 170,000µF over the typical telecom operating voltage range.

$$I_{TEST}\ (A) = C_{LOAD,MAX}\ (F) \times 220mV / 80ms$$

Since the minimum intended V_{IN} for the application results in the lowest I_{TEST}, during the load-probe test, this $V_{IN,MIN}$ should be used to set the R_{LP}. This voltage will likely be near $V_{ON,FALLING}$ or V_{OFF} for the application.

$$R_{TEST}(\Omega) = V_{IN,MIN} / I_{TEST} = V_{IN,MIN} \times 80ms / (C_{LOAD(MAX)} \times 220mV)$$

Example: V_{IN} operating range = 36V to 72V, C_{LOAD} = 10,000µF. First, find the $R_{TEST,}$ which will guarantee a successful test of the load.

$$R_{LP} = 36V \times 80ms / (10,000\mu F \times 220mV) = 1,309\Omega \Rightarrow 1.30k\Omega \pm 1\%$$

Next, evaluate the R_{LP} at the maximum operating voltage to verify that it will not exceed the 1A current limit for the load-probe test:

$$I_{TEST,MAX} = V_{IN,MAX} / R_{LP} = 72V / 1.30k\Omega = 55.4mA$$

If the $C_{LOAD(MAX)}$ is increased to 170,000µF, the test current will approach the limit. In this case, R_{TEST} will be a much lower value and must include the internal switch resistance. To find the external series resistor value that will guarantee a successful test at the lowest supply voltage, the maximum value for the load-probe switch on-resistance of 11Ω should be used:

$$R_{LP,TOT} = 36V \times 80ms / (170,000\mu F \times 220mV) = 77\Omega = 11\Omega + R_{LP}$$

$$R_{LP} = 77\Omega - 11\Omega = 66\Omega \Rightarrow 66.5\Omega \pm 1\%$$

Again R_{LP} must be evaluated at the maximum operating voltage to verify that it will not exceed the 1A current limit for the load-probe test. In this case, the minimum value for the load-probe switch on-resistance of 6Ω should be used:

$$I_{TEST,MAX} = V_{IN,MAX} / R_{LP,TOT} = 72V / (66.5\Omega + 6\Omega) = 993mA$$

-48V Hot-Swap Controllers with V_{IN} Step Immunity and No R_{SENSE}

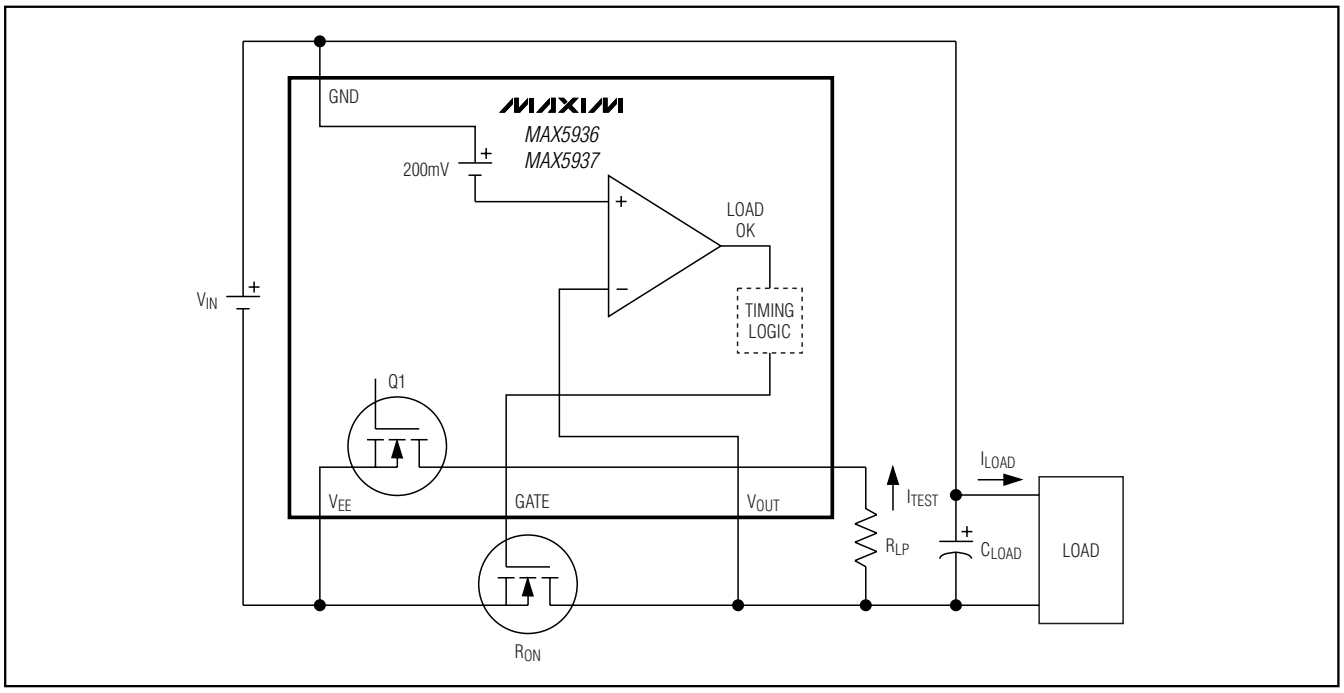

Figure 14. Load Probe Functional Diagram

Adjusting the V_{OUT} Slew Rate

The default slew rate is set internally for 9V/ms. The slew rate can be reduced by placing an external capacitor from the drain of the power MOSFET to the GATE output of the MAX5936/MAX5937. Figure 15 shows a graph of Slew Rate vs. C_{SLEW}. This graph shows that for C_{SLEW} < 4700pF there is very little effect to the addition of external slew-rate control capacitance. This is intended so the GATE output can drive large MOSFETs with significant gate capacitance and still achieve the default slew rate. To select a slew-rate control capacitor, go into the graph with the desired slew rate and find the value of the miller capacitance. When C_{SLEW} > 4700pF, SR and C_{SLEW} are inversely related. Given the desired slew rate, the required C_{SLEW} is found as follows:

$$C_{SLEW}(nF) = 23 / SR\ (V/ms)$$

From the data sheet of the power MOSFET find the reverse transfer capacitance (gate-to-drain capacitance) above 10V. If the reverse transfer capacitance of the external power MOSFET is 5% or more of C_{SLEW}, then it should be subtracted from C_{SLEW} in the equation above.

Figure 16 gives an example of the external circuit for controlling slew rate. Depending on the parasitics associated with the selected power MOSFET, the addition of C_{SLEW} may lead to oscillation while the MOSFET and GATE control are in the linear range. If this is an issue, an external resistor, R_{GATE}, in series with the gate of the MOSFET is recommended to prevent possible oscillation. It should be as small as possible, e.g., 5Ω to 10Ω, to avoid impacting the MOSFET turn-off performance of the MAX5936/MAX5937.

Layout Guidelines

To benefit from the temperature compensation designed into the MAX5936/MAX5937, the part should be placed as close as possible to the power MOSFET that it is controlling. The V_{EE} pin of the MAX5936/ MAX5937 should be placed close to the source pin of the power MOSFET and they should share a wide trace. A common top layer plane would service both the thermal and electrical requirements. The load-probe current must be taken into account. If this current is high, the layout traces and current-limiting resistor must be sized appropriately. Stray inductance must be minimized in the traces of the overall layout of the hot-swap controller, the power MOSFET, and the load capacitor. Starting from the board contacts, all high-current traces should be short, wide, and direct. The potentially high pulse current pins of the MAX5936/MAX5937 are GATE (when pulling GATE low),

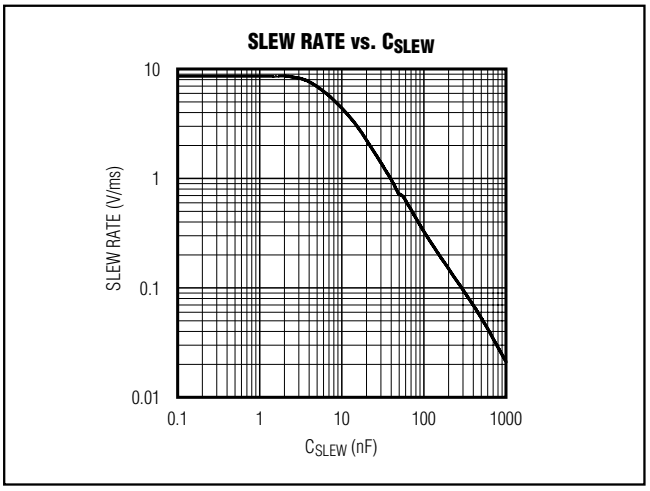

Figure 15. MAX5936/MAX5937 Slew Rate vs. C_{SLEW}

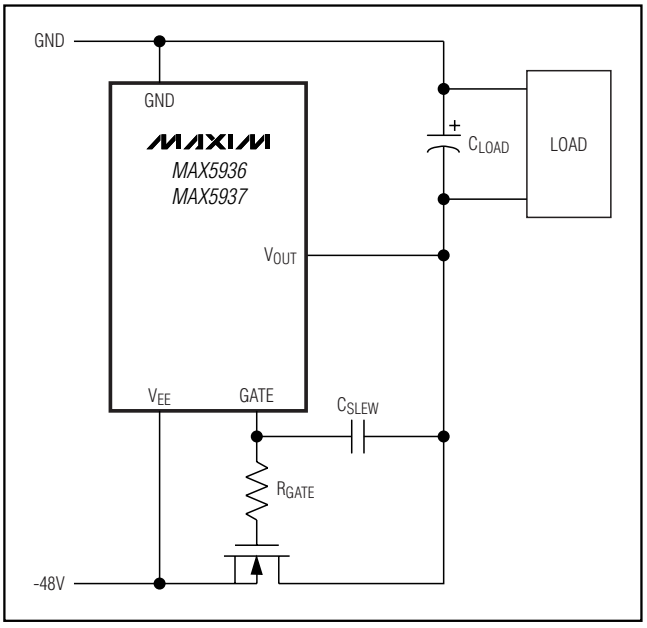

Figure 16. Adjusting the MAX5936/MAX5937 Slew Rate

load-probe, and V_{EE}. Because of the nature of the hot-swap requirement, no decoupling capacitor is recommended for the MAX5936/MAX5937. Because there is no decoupling capacitor, stray inductance can result in excessive ringing at the GND pin during power-up or during very rapid V_{IN} steps. This should be examined in every application design since ringing at the GND pin may exceed the absolute maximum supply rating for the part.

Input Transient Protection

During hot plug-in/unplug and fast V_{IN} steps, stray inductance in the power path can cause voltage ringing above the normal input DC value, which may exceed the absolute maximum supply rating. An input transient such as that caused by lightning can also put a severe transient peak voltage on the input rail. The following techniques are recommended to reduce the effect of transients:

1) Minimize stray inductance in the power path using wide traces and minimize loop area including the power traces and the return ground path.
2) Add a high-frequency (ceramic) bypass capacitor on the backplane as close as possible to the plug-in connector (Figure 17).
3) Add a 1kΩ resistor in series with the MAX5936/MAX5937's GND pin and a 0.1µF capacitor from GND to V_{EE} to limit transient current going into this pin.

Appendix A

GATE Cycles

The power-up GATE cycle and the step GATE cycle are quite similar but have distinct differences. Understanding these differences may clarify application issues.

GATE Cycle During Power-Up

The power-up GATE cycle occurs during the initial power-up of the MAX5936/MAX5937 and the associated power MOSFET and load. The power-up GATE cycle can result in full enhancement or in a fault (all voltages are relative to V_{EE}).

Power-Up to Full Enhancement:

1) At the beginning of the power-up sequence to the start of the power-up GATE cycle, the GATE is held at V_{EE}. Following a successful completion of the load-probe test, GATE is held at V_{EE} for an additional 350µs and then is allowed to float for 650µs. At this point, the GATE begins to ramp with 52µA charging the gate of the power MOSFET. [GATE turn-on]
2) When GATE reaches the gate threshold voltage of the power MOSFET, V_{OUT} begins to ramp down toward V_{EE}. [V_{OUT} ramp]
3) When V_{OUT} ramps below 72% V_{CB}, the GATE is rapidly pulled to full enhancement and the power-up GATE cycle is complete. 1.26ms after GATE is pulled to full enhancement, PGOOD will assert. [Full enhancement]

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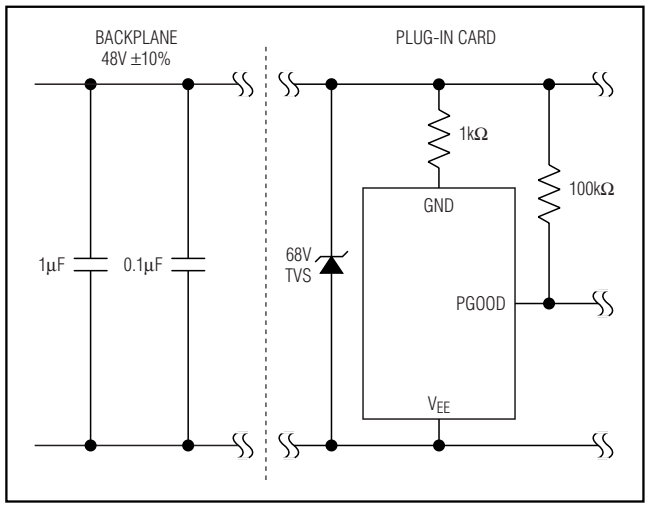

Figure 17. Protecting the MAX5936/MAX5937 Input from High-Voltage Transients

Power-Up to Fault Management:

1) Same as step 1 above. [GATE turn-on]
2) Same as step 2 above. [V_{OUT} ramp]
3) GATE ramps to 90% of full enhancement while V_{OUT} remains above 72% V_{CB}, at which point the GATE is rapidly pulled to V_{EE} and fault management is initiated. [Fault management]

GATE Cycle During V_{IN} Step

A step GATE cycle occurs only after a successful power-up GATE cycle to full enhancement occurs and as a result of a positive V_{IN} step (all voltages are relative to V_{EE}).

Step to Full Enhancement:

1) A V_{IN} step occurs resulting in STEP_MON rising above $STEP_{TH}$ before V_{OUT} rises above V_{SC}. [Step detection]
2) After a step is detected, V_{OUT} rises above V_{SC} in response to the step. When V_{OUT} rises above V_{SC}, GATE is immediately pulled to V_{EE}, rapidly turning off the power MOSFET. GATE is held at V_{EE} for 350µs to dampen any ringing. Once GATE is pulled to V_{EE}, the gate cycle has begun and STEP_MON can safely drop below $STEP_{TH}$ and successfully complete a step GATE cycle to full enhancement without initiating fault management. [GATE pulldown]
3) Following the 350µs of GATE pulldown, GATE is allowed to float for 650µs. At this point, the GATE begins to ramp with 52µA charging the gate of the power MOSFET. [GATE turn-on]
4) When GATE reaches the gate threshold voltage of the power MOSFET, V_{OUT} begins to ramp down toward the new lower V_{EE}. In the interval where GATE is below the MOSFET threshold, the MOSFET is off and V_{OUT} will droop depending on the RC time constant of the load. [V_{OUT} ramp]
5) When V_{OUT} ramps below 72% V_{CB}, the GATE pulls rapidly to full enhancement and the step GATE cycle is complete. If STEP_MON remains above $STEP_{TH}$ when GATE has ramped to 90% of full enhancement and V_{OUT} remains above 72% of V_{CB}, GATE remains at 90% and will not be pulled to full enhancement. In this condition, if V_{OUT} drops below 72% of V_{CB} before STEP_MON drops below $STEP_{TH}$, GATE is rapidly pulled to full enhancement and the step GATE cycle is complete. PGOOD remains asserted throughout the step GATE cycle. [Full enhancement]

Step to Fault Management:

1) Same as step 1 above. [Step detection]
2) Same as step 2 above. [GATE pulldown]
3) Same as step 3 above. [GATE turn-on]
4) Same as step 4 above. [VOUT ramp]
5) If STEP_MON is below $STEP_{TH}$ when GATE ramps to 90% of full enhancement and V_{OUT} remains above 72% V_{CB}, GATE is rapidly pulled to V_{EE}. Fault management is initiated and PGOOD is deasserted. If STEP_MON is above $STEP_{TH}$ when GATE ramps to 90% of full enhancement and V_{OUT} remains above 72% of V_{CB}, GATE remains at 90%. It will not be pulled to full enhancement nor will it be pulled to V_{EE}. In this condition, if V_{OUT} drops below 72% of V_{CB} before STEP_MON drops below $STEP_{TH}$, GATE is rapidly pulled to full enhancement and a fault is avoided. Conversely, if STEP_MON drops below $STEP_{TH}$ first, the GATE is rapidly pulled to V_{EE}, fault management is initiated, and PGOOD is deasserted. [Fault management]

It should be emphasized that while STEP_MON remains above $STEP_{TH}$ the current fault management is blocked. During this time it is possible for there to be multiple events involving V_{OUT} rising above V_{SC} then those falling below 75% V_{CB}. In each of these events, when V_{OUT} rises above V_{SC}, a full GATE cycle is initiated where GATE is first pulled low then allowed to ramp up. Then finally, when V_{OUT} conditions are met, it will be fully enhanced.

GATE Output

GATE is a complex output structure and its condition at any moment is dependent on various timing sequences in response to multiple inputs. A diode to V_{EE} prevents negative excursions. For positive excursions, the states are:

1) Power-off with 2V clamp.
2) 10Ω pulldown to V_{EE}.
   a. Continuous during startup delay and during fault conditions.
   b. Pulsed following detected step or OV condition.
3) Floating with 15V clamp. [Prior to GATE ramp]
4) 47µA current source with 15V clamp. [GATE ramp]
5) Pullup to internal 10V supply with 15V clamp. [Full enhancement]

Appendix B

Step Monitor Component Selection Analysis

As mentioned previously in the *Selecting Resistor and Capacitor for Step Monitor* section, the AC response from V_{IN} to V_{OUT} is dependent on the parasitics of the load. This is especially true for the load capacitor in conjunction with the power MOSFET's $R_{DS(ON)}$. The load capacitor (with parasitic ESR and LSR) and the power MOSFET's $R_{DS(ON)}$ can be modeled as a heavily damped second-order system. As such, this system functions as a bandpass filter from V_{IN} to V_{OUT} limiting the ability of V_{OUT} to follow the V_{IN} ramp. STEP_MON lags the V_{IN} ramp with a first-order RC response, while V_{OUT} lags with an overdamped second-order response.

Given a positive V_{IN} ramp with ramp rate of dV/dt, the approximate response of V_{OUT} to V_{IN} is:

$$V_{OUT}(t) = (dV/dt) \times \tau_C \times (1-e^{(-t / \tau L,eqv)}) + R_{DS(ON)} \times I_{LOAD} \quad \text{(Equation 1)}$$

where $\tau_C = C_{LOAD} \times R_{DS(ON)}$.

Equation 1 is a simplification for the overdamped second-order response of the load to a ramp input, $\tau_C = C_{LOAD} \times R_{DS(ON)}$, and corresponds to the ability of the load capacitor to transfer dV/dt current to the fully enhanced power MOSFET's $R_{DS(ON)}$. The equivalent time constant of the load ($\tau_{L,eqv}$) accounts for the parasitic series inductance and resistance of the capacitor and board interconnect. Determine $\tau_{L,eqv}$ empirically with a few tests to characterize the load dynamic response to V_{IN} ramps.

Similarly, the response of STEP_MON to a V_{IN} ramp is:

$$V_{STEP\_MON}(t) = (dV/dt) \times \tau_{STEP} \times (1-e^{(-t / \tau STEP)}) + 10\mu A \times R_{STEP\_MON} \quad \text{(Equation 2)}$$

where $\tau_{STEP} = R_{STEP\_MON} \times C_{STEP\_MON}$.

For proper step detection, V_{STEP_MON} must exceed $STEP_{TH}$ prior to V_{OUT} reaching V_{SC} or within 1.4ms of V_{OUT} reaching V_{CB} (or overall V_{IN} ramp rates anticipated in the application). It is impossible to give a fixed set of design guidelines that rigidly apply over the wide array of applications that use the MAX5936/MAX5937. There are, however, limiting conditions and recommendations that should be observed.

One limiting condition that must be observed is to ensure that the STEP_MON time constant, τ_{STEP}, is not so low that at the lowest ramp rate, the anticipated $STEP_{TH}$ cannot be obtained. The product (dV/dt) x τ_{STEP} = $\tau_{STEP\_MON,MAX}$, is the maximum differential voltage at STEP_MON if the V_{IN} ramp were to continue indefinitely. A related condition is setting the STEP_MON voltage below $STEP_{TH}$ with adequate margin, ΔV_{STEP_MON}, to accommodate the tolerance of both I_{STEP_OS} (±8%) and R_{STEP_MON}. In determining τ_{STEP_MON}, use the 9.2µA limit to ensure sufficient margin with worst-case I_{STEP_OS}.

The margin of V_{OUT} (with respect to V_{SC} and V_{CB}) is set when V_{SC} and V_{CB} were selected from the three available ranges. This margin may be lower at one of the temperature extremes and if so, that value should be used in the following discussion. These margins will be called ΔV_{CB} and ΔV_{SC} and they represent the minimum V_{OUT} excursion required to trip the respective fault. R_{STEP_MON} is typically set to 100kΩ ±1%. This gives a ΔV_{STEP_MON} of 0.25V, a worst-case low of 0.16V, and a worst-case high of 0.37V. In finding τ_{STEP} in the equation below, use ΔV_{STEP_MON} = 0.37V to ensure sufficient margin with worst-case I_{STEP_OS}.

To set τ_{STEP} to block all V_{CB} and V_{SC} faults for any ramp rate, find the ratio of ΔV_{STEP_MON} to ΔV_{CB} and choose τ_{STEP} so:

$$\tau_{STEP} = 1.2 \times \tau_C \times \Delta V_{STEP\_MON} / \Delta V_{CB}$$

and since R_{STEP_MON} = 100kΩ:

$$C_{STEP\_MON} = \tau_{STEP} / R_{STEP\_MON} = \tau_{STEP} / 100k\Omega$$

After the first-pass component selection, if sufficient timing margin exists, it is possible but not necessary to lower R_{STEP} below 100kΩ to reduce the sensitivity of STEP_MON to V_{IN} noise.

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Verification of the Step Monitor Timing

It is prudent to verify conclusively that all circuit-breaker and short-circuit faults will be blocked for all ramp rates. To do this, some form of graphical analysis is recommended but first, find the value of $\tau_{L,eqv}$ of the load by a series of ramp tests as indicated earlier. These tests include evaluating the load with a series of V_{IN} ramps of increasing ramp rates and monitoring the rate of V_{OUT} rise during the ramp. Each V_{IN} ramp should have a constant slope. The V_{OUT} response data must be taken only during the positive ramp. Data taken after V_{IN} has leveled off at the new higher value must not be used.

Figure 18 shows the load in parallel with the load capacitor, C_{LOAD}, and the parallel connection in series with the power MOSFET, which is fully enhanced with V_{GS} = 10V. The objective is to determine $\tau_{L,eqv}$ from the V_{OUT} response.

Figure 19 shows the general response of V_{OUT} to a V_{IN} ramp over time t. Equation 1 gives the response of V_{OUT} to a ramp of dV/dt. The product (dV/dt) x τ_C = ΔV_{OUT}(max) or the maximum V_{OUT} voltage differential if the V_{IN} ramp were to continue indefinitely. The parameter of interest is ΔV_{OUT} due to the ramp dV/dt, thus it is necessary to subtract the DC shift in V_{OUT} due to the load resistance. For some loads, which are relatively independent of supply voltage, this may be insignificant.

$$V_{OUT}(t) = V_{OUT}(t) - R_{DS(ON)} \times I_{LOAD}$$

where I_{LOAD} is a function of the V_{OUT} level that should be determined separately with DC tests.

At any time (t) the ΔV_{OUT} fraction of ΔV_{OUT}(max) is:

$$\Delta V_{OUT}(t) / [(dV/dt) \times \tau_C] = (1-e^{(-t / \tau L,eqv)})$$

If $V_{OUT}(t)$ is measured at time t, then the equivalent time constant of the load is found from:

$$\tau_{L,eqv} = -t / \ln(1 - \Delta V_{OUT} / [(dV/dt) \times \tau_C])$$

As mentioned earlier, several measurements of ΔV_{OUT} at times t1, t2, t3, and t4 should be made during the ramp. Each of these may result in slightly different values of $\tau_{L,eqv}$ and all values should then be averaged. In making the measurements, the V_{IN} ramp duration should be such that ΔV_{OUT} reaches 2 or 3 times the selected ΔV_{SC}. The ramp tests should include three ramp rates: $\Delta V_{SC} / \tau_C$, 2 x $\Delta V_{SC} / \tau_C$ and 4 x $\Delta V_{SC} / \tau_C$. The values of $\tau_{L,eqv}$ may vary over the range of slew rates due to measurement error, nonlinear dynamics in the load, and due to the fact that Equation 1 is a simplification from a higher order dynamic system. The resulting range of $\tau_{L,eqv}$ values should be used to validate the performance of the final design.

Having τ_C, $\tau_{L,eqv}$, R_{STEP}, and C_{STEP} in a graphical analysis using Equation 1 and Equation 2 can verify the step monitor function by displaying the relative timing of t_{CB}, t_{STEP}, and t_{SC}, which are the times when V_{CB}, V_{STEP_MON}, and V_{SC} voltage thresholds are exceeded. A simple spreadsheet for this purpose can be supplied by Maxim upon request. Figures 20, 21, and 22 graphically verify a particular solution over 3 decades of V_{IN} ramp rates. In addition, Figure 22 verifies that this solution will block all circuit-breaker and short-circuit faults for even the lowest V_{IN} ramp that will cause V_{OUT} to exceed V_{CB}.

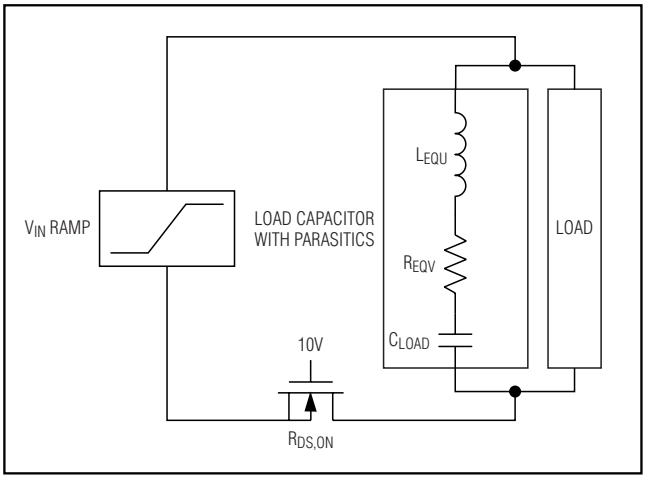


Figure 18. V_{IN} Ramp Test of Load

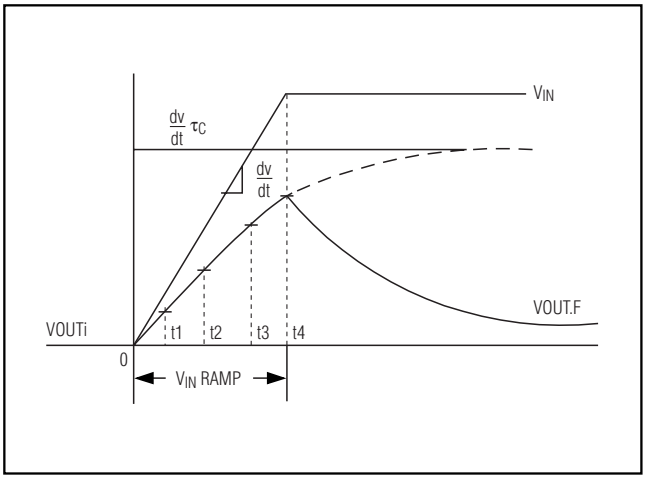


Figure 19. General Response of V_{OUT} to a V_{IN} Ramp

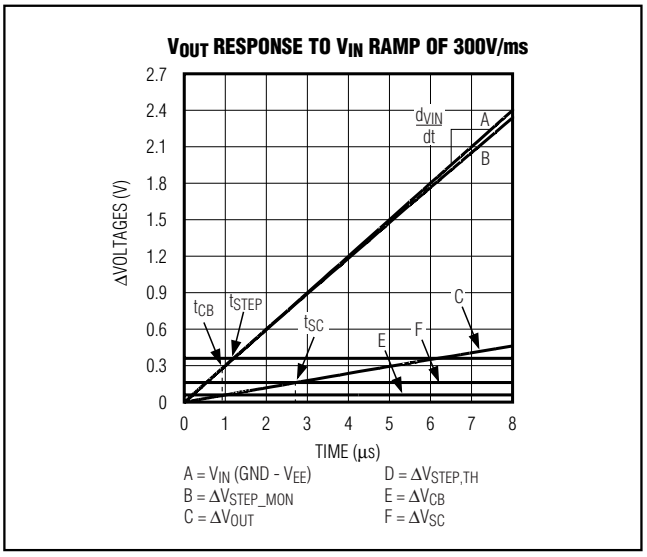


Figure 20. V_{OUT} Response to V_{IN} Ramp of 300V/ms

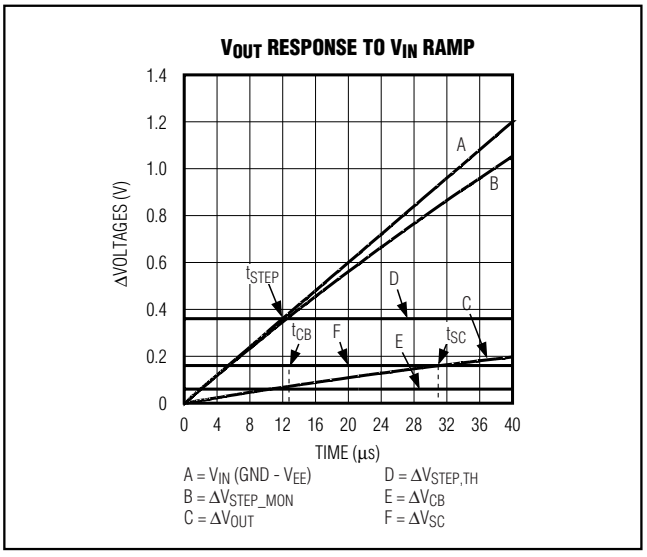


Figure 21. V_{OUT} Response to V_{IN} Ramp of 30V/ms

Chip Information

TRANSISTOR COUNT: 2320

PROCESS: BiCMOS

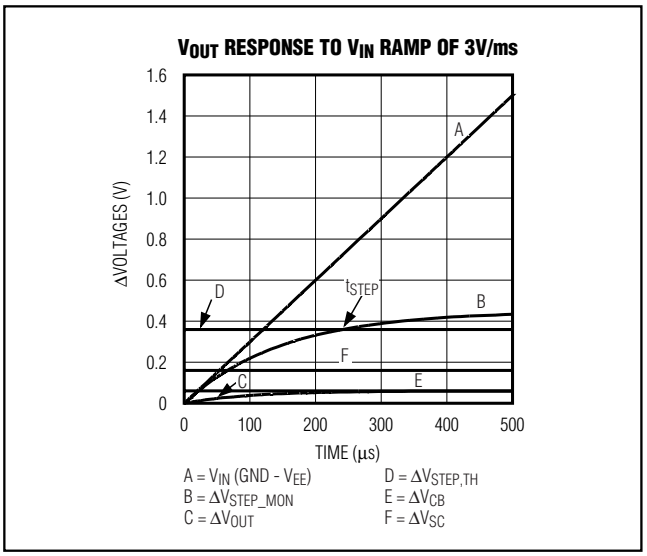


Figure 22. V_{OUT} Response to V_{IN} Ramp of 3V/ms

-48V Hot-Swap Controllers with V_{IN} Step Immunity and No R_{SENSE}

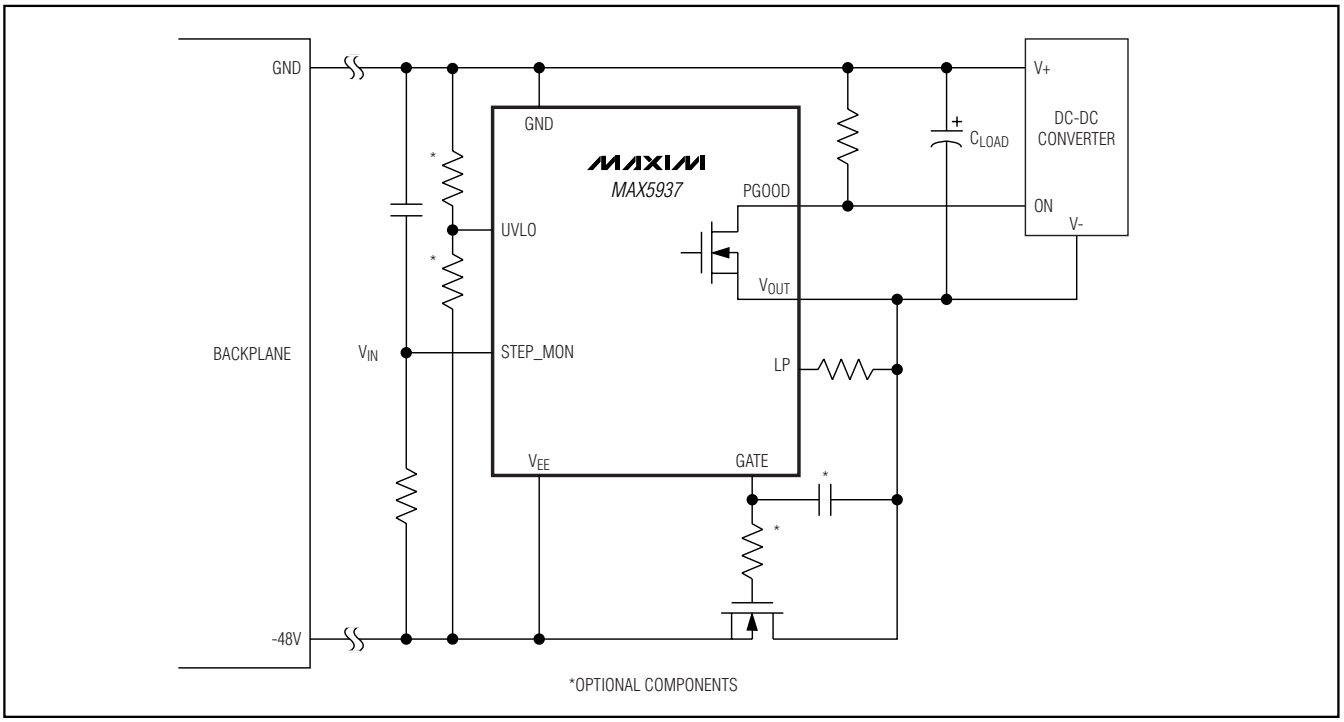
Timing Table

NAME	SYMBOL	TYPICAL TIME (s)
Power-Up Delay	t_{ONDLY}	220m
Load Probe Test Timeout	t_{LP}	220m
Load Probe Retry Time	t_{LP_OFF}	3.5
PGOOD ($\overline{PGOOD}$) Assertion Delay Time	t_{PGOOD}	1.26m
Autoretry Delay	t_{RETRY}	3.5
Circuit-Breaker Glitch Rejection	t_{CB_DLY}	1.4m
UVLO Glitch Rejection	t_{REJ}	1.5m
GATE Pulldown Pulse Following a V_{IN} step	—	350µ
GATE Low After a V_{IN} Step, Prior to Ramp	—	1m

Selector Guide

PART	CIRCUIT-BREAKER THRESHOLD (mV)	FAULT MANAGEMENT	PGOOD ASSERTION
MAX5936LA	100	Latch	Low
MAX5936LB	200	Latch	Low
MAX5936LC	400	Latch	Low
MAX5936LN	No circuit breaker	Latch	Low
MAX5936AA	100	Autoretry	Low
MAX5936AB	200	Autoretry	Low
MAX5936AC	400	Autoretry	Low
MAX5937LA	100	Latch	High
MAX5937LB	200	Latch	High
MAX5937LC	400	Latch	High
MAX5937LN	No circuit breaker	Latch	High
MAX5937AA	100	Autoretry	High
MAX5937AB	200	Autoretry	High
MAX5937AC	400	Autoretry	High

Typical Operating Circuit



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

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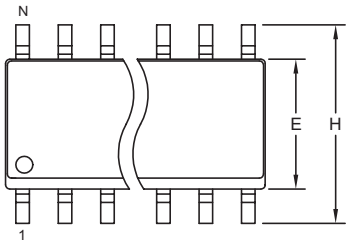
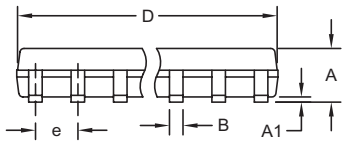


TOP VIEW

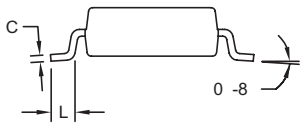
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1